REMARKS

Claims 1-45 are pending in the present application. Claims 1, 8, 17, 23, 33 and 37 are herein amended. Applicants respectfully that no new matter is added as a result of the amendments presented herein. Applicants respectfully request reconsideration of the present application in view of the remarks presented herein.

35 USC § 101

Claims 1, 17, 18, 23, 33 and 37 are rejected under 35 USC § 101, as allegedly being directed to non-statutory subject matter. The rejection alleges that Claims 1 and 18 fail to recite a "physical transformation." Applicants respectfully traverse. Applicants respectfully assert that Claims 1 and 18 recite, "modifying" an instruction segment, e.g., a pattern of bits, within a computer processor. As is well understood in the art, and as described in the present application, a bit pattern represents physical electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. Hence, bits, bit patterns and "instruction segment(s)" represent physical entities as recited. Furthermore, Applicants respectfully assert that the recited "modifying" of the recited bit patterns represents a physical transformation.

In addition, the rejection alleges, "the claim is not useful because no substantial practical application can be found in the claim. Applicants respectfully traverse. Applicants respectfully assert that 35 USC § 101 does not require a "practical application" to be recited in the claims. Applicants respectfully assert that the present claimed invention is useful, and would be understood as useful to one or ordinary skill in the art Executing instructions on a processor is the foundation of application software and operating system software that supports it. Applicants respectfully assert that such software exists globally and is useful.

For these reasons, Applicants respectfully assert that Claims 1 and 18 fully comply with 35 USC § 101, and that the rejections under 35 USC § 101 are overcome.

Claims 17, 23, 33 and 37 are rejected under similar arguments. Applicants respectfully assert that these Claims overcome the 35 USC § 101 rejections for at least the rationale previously presented.

35 U.S.C. § 102

Claims 1-5, 8, 9-14, 17, 18, 20-23 and 34-36 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Nunomura (US 6,871,274, "Nunomura"). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments of the present invention as recited in Claims 1-5, 8, 9-14, 17, 18, 20-23 and 34-36 are patentable over Nunomura.

With respect to Claim 1, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "fetching a first machine language instruction" as recited by Claim 1. Applicants respectfully assert that the rejection improperly equates the taught "compressed instruction code" with the recited machine language instruction.

In contrast, Nunomura teaches "a compressed instruction code" (column 2, lines 2-3, *inter alia*). In addition, Nunomura teaches that such "compressed instruction code" is accessed by "an instruction code conversion apparatus" (column 2, lines 1-2, *inter alia*) and not by an "instruction decode unit" (column 5 lines 6-20), as are other machine language instructions.

Further, Nunomura teaches, "an instruction code conversion apparatus converts a first code to a second code longer in bit length than the first code to

create an instruction code" (column 2, lines 17-19, *inter alia*). In teaching that an "instruction code" is created, Nunomura teaches that the taught "first code," also known as a "compressed instruction code," is not an "instruction code." Consequently, Applicants respectfully assert that Nunomura teaches that the "compressed instruction code" is not a machine language instruction. Applicants respectfully further assert that one of ordinary skill in the art would not understand the taught "compressed instruction code" to teach or fairly suggest the recited "machine language instruction" as recited by Claim 1.

Still further, Nunomura teaches that the "compressed instruction code" is "unrecognizable as an instruction code." (column 7 lines 30-37).

For these reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 1, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "modifying said instruction segment to form a second machine language instruction" as recited by Claim 1.

Claim 1 recites that the instruction segment is part of a first machine language instruction. Even if, *arguendo*, the taught "compressed instruction

code" suggests a machine language instruction, Nunomura fails to teach or fairly suggest the limitation of "modifying said instruction segment" as recited by Claim 1.

As taught by Nunomura, a segment of the "compressed instruction code" is replaced by a second code "longer in bit length than the first code" (column 2 lines 18-19). For example, Figure 4 shows a four-bit "index" mapping into a 24 bit op code. Applicants respectfully assert that a code segment "longer in bit length than the first code" as taught by Nunomura, cannot be the recited "instruction segment" that is part of the recited first machine language instruction. Applicants respectfully assert that an "instruction segment" as recited by Claim 1 cannot simultaneously be both four bits and 24 bits long. Further, Applicants respectfully assert that an alleged first machine language instruction taught as 16 bits in length cannot comprise an "instruction segment" of 24 bits in length.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 8, 17, 33 and 37 are rejected under the same rationale as applied to Claim 1. Applicants respectfully assert that Claims 8, 17, 33 and 37

overcome the rejections of record for at least the rationale previously presented with respect to Claim 1, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 2-7, 9-16, 18-22, 34-36 and 38-45 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 2, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "substitut(ing) a bit pattern of a subset of said instruction segment" as recited by Claim 2. In contrast, Nunomura teaches "substituting" more bits than an instruction segment contains. In this manner, Nunomura actually teaches away from the recited limitation of substituting a subset of bits of an instruction segment, as recited by Claim 2.

For this additional reason, Applicants respectfully assert that Claim 2 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 4, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "executing microcode" as recited by Claim 4. Applicants respectfully assert that

Nunomura is completely silent as to such recited microcode. Applicants respectfully note that Figure 4, cited in rejecting Claim 4, refers to compressed instructions and instruction codes. Such codes do not teach or fairly suggest microcode, as used in the art, as explained in the present application and as recited in the instant claim.

For this additional reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 10, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "advancing a queue structure to a next entry storing instruction modification information in said memory" as recited by Claim 10. Applicants respectfully assert that Nunomura is completely silent as to such queue structures. Applicants respectfully note that Figure 2, cited in rejecting Claim 10, refers to a table mapping an index code to a non-compressed instruction code. Such a table does not teach or fairly suggest a queue, as used in the art, as explained in the present application and as recited in the instant claim.

For this additional reason, Applicants respectfully assert that Claim 10 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 11, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "advancing a pointer to indicate said next entry storing instruction modification information in said (queue)" as recited by Claim 11. Applicants respectfully assert that Nunomura is completely silent as to such queue structures or queue pointers. Applicants respectfully note that Figure 2, cited in rejecting Claim 11, refers to a table mapping an index code to a non-compressed instruction code. Such a table does not teach or fairly suggest a queue or queue pointer or advancing a queue pointer, as used in the art, as explained in the present application and as recited in the instant claim.

For this additional reason, Applicants respectfully assert that Claim 11 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 34, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "decoding said trigger pattern to identify said portion of said machine language instruction" as recited

by Claim 34. Applicants respectfully assert that Nunomura is completely silent as to a trigger pattern identifying a portion of a machine language instruction. Applicants respectfully note that Figure 2, cited in rejecting Claim 34, refers to a table mapping an index code to a non-compressed instruction code. Such a table does not teach or fairly suggest identifying a portion of an instruction for modification, as used in the art, as explained in the present application and as recited in the instant claim.

In contrast, Nunomura teaches that the same portion of a compressed instruction code, e.g., the index in Figure 4, is always the portion changed. Hence, there is no need in Nunomura to decode anything in order to determine which portion of a compressed instruction code is to be substituted, and therefore Nunomura fails to teach or fairly suggest "decoding said trigger pattern to identify said portion of said machine language instruction" as recited by Claim 34.

For this additional reason, Applicants respectfully assert that Claim 34 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

35 U.S.C. § 103

Claims 6, 7, 16, 23-27, 32, 38 and 39 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Nunomura (US 6,871,274, "Nunomura") in view of Rim (US 6,202,143, "Rim"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claims 6, 7, 16, 23-27, 32, 38 and 39 are patentable over Nunomura in view of Rim.

With respect to Claims 6, 7, 16, 23-27, 32, 38 and 39, Applicants respectfully assert that the proposed manner of combination of Nunomura in view of Rim is not supported by the references. Rim teaches multiple program memories for storing multiple sizes of instruction words, and that the multiple program memories "preferably have different (bus) widths" (Abstract). In contrast, Nunomura teaches a single memory with a single bus size. Applicants respectfully assert that one of ordinary skill in the art would not be motivated to combine these references in the manner suggested because of the complexity of Rim in contrast to the relative simplicity of Nunomura.

For this reason, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim does not motivate the claimed subject matter, and that all rejections dependent upon this combination of references

are overcome. The rejection proposes, as motivation for the proposed manner of combination, that one of ordinary skill would be motivated to increase the adaptability of Nunomura to accept long instruction words. Applicants respectfully traverse. There is no teaching in the prior art as to the desirability of modifying Nunomura to accept VLIW instructions. Moreover, Nunomura fails to teach or fairly suggest the multiple instruction units necessary to process a VLIW instruction. Thus, even if Nunomura was modified in view of Rim to "recognize() ... specific instruction type with corresponding width of the Rim's VLIW," the proposed combination would be unable to execute such VLIW instructions. Applicants respectfully assert that one of ordinary skill in the art would not be motivated to modify Nunomura in view of Rim, in the manner proposed by the rejection, to "recognize" VLIW instructions in spite of a lack of capability to execute such instructions.

For this additional reason, Applicants respectfully assert that the proposed manner of combination of Nunomura in view of Rim is is not suggested by the cited references, and that all rejections dependent upon this combination of references are overcome. Applicants respectfully solicit allowance of Claims 6, 7, 16, 23-27, 32, 38 and 39.

Further, Nunomura teaches a method of storing instructions in a compressed format. In contrast, Rim teaches a method of expanding a complete

uncompressed instruction with meaningless filler (a "NOP" or no operation instruction) to fill a wide bus. Applicants respectfully assert that, in consideration of the whole of the teachings of Nunomura and Rim, one of ordinary skill in the art would not be motivated to modify a decompression process with a process that stuffs meaningless filler into an instruction word. Moreover, Nunomura has no need for the filler methods of Rim, as Nunomura has a single bus and a single bus width.

For this further reason, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim is improper, and that all rejections dependent upon this combination of references are overcome. Applicants respectfully solicit allowance of Claims 6, 7, 16, 23-27, 32, 38 and 39.

With respect to Claims 6, 7, 16, 23-27, 32, 38 and 39, Applicants respectfully assert that Nunomura fails to teach or fairly suggest the limitation of "fetching a first machine language instruction" as recited by the instant Claims, for at least the rationale previously presented with respect to Claim 1. As Rim fails to correct this deficiency of Nunomura, Applicants respectfully assert that Claims 6, 7, 16, 23-27, 32, 38 and 39 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 2-7, 9-16, 34-36 and 38-45 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 6, Applicants respectfully assert that Nunomura in view of Rim fails to teach or fairly suggest the limitation of "wherein said first machine language instruction comprises a very long instruction word" as recited by Claim 6. Applicants are unclear as to what format a compressed instruction code might have under the modification proposed by the rejection, but respectfully assert that such a compressed instruction code would not be a very long instruction word as specifically recited by Claim 6.

While Nunomura in view of Rim may allegedly teach some form of manipulating a first bit pattern to produce a second bit pattern, wherein the second bit.pattern is a VLIW instruction, the recited limitation refers to accessing a VLIW instruction, e.g., the allegedly taught first bit pattern must be a VLIW instruction. Applicants understand that it is the intention of Nunomura is to reduce the size of such compressed instruction codes. Hence, Nunomura teaches away from the recited fetching VLIW machine language instructions as recited by Claim 6..

For this additional reason, Applicants respectfully assert that Claim 6 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 23, Applicants respectfully assert that Nunomura in view of Rim fails to teach or fairly suggest modifying a "very long instruction word" as recited by Claim 23. As described previously with respect to Claim 6, Nunomura in view of Rim may allegedly teach some form of manipulating a first bit pattern to produce a VLIW instruction. However, Applicants respectfully assert that the first bit pattern taught by Nunomura in view of Rim is not a VLIW instruction, as recited by Claim 23.

For this additional reason, Applicants respectfully assert that Claim 23 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 24-32 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

Claims 28-31, 40-44 and 45 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Nunomura (US 6,871,274, "Nunomura") in

view of Rim (US 6,202,143, "Rim") and further in view of Ebicioglu et al (US 6,112,299, "Ebicioglu"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claims 28-31, 40-44 and 45 are patentable over Nunomura in view of Rim and further in view of Ebicioglu.

For at least the rationale previously presented with respect to Claims 6, 7, 16, 23-27, 32, 38 and 39, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim is improper, and that all rejections dependent upon this combination of references are overcome. For this reason, Applicants respectfully assert that Claims 28-31, 40-44 and 45 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 28-31, 40-44 and 45 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

With respect to Claim 28, Applicants respectfully assert that Nunomura in view of Rim fails to teach or fairly suggest the limitation of said trigger pattern identifies an arithmetic logic unit segment" as recited by Claim 28. As recited by Claim 23, from which Claim 28 depends, the recited "trigger pattern initiate(s) modification of a segment of said very long instruction word."

While Ebicioglu may imply that various portions of a VLIW may be identified, Ebicioglu further teaches, "each parcel 510 occupies specific bit positions and controls those hardware units hard-wired to those positions" (column 11 lines 15-36). By teaching hardware units hard-wired to specific bit positions, Ebicioglu teaches away from embodiments of the present invention that recite a "trigger pattern identifies an arithmetic logic unit segment" as recited by Claim 28.

For this additional reason, Applicants respectfully assert that Claim 28 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

CONCLUSION

Claims 1-45 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the amendments and remarks presented herein.

Applicants have reviewed the following references that were cited but not relied upon and do not find these references to show or suggest the present claimed invention: US 6,230,260 and 6,658,551.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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